REMARKS

This paper is responsive to Non-Final Office Action dated May 12, 2006. Claims 1-19 were examined. New claims 20-21 are added. All rejections are respectfully traversed.

Rejection for Obviousness-type Double Patenting

Claims 1-19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 of Applicant's prior U.S. Patent No. 6,507,862 (hereafter the '862 patent). While Applicants are happy to consider the propriety of any obviousness-type double patenting rejection once subject matter is indicated to be otherwise allowable, terminal disclaimer would appear premature at this point.

Though the Office casts a wide net in its assertion of obviousness-type double patenting (claims 1-19), there is really no clear basis for assertion of the doctrine with respect to most, if not all, of the present claims. Differences between the inventions defined by relied upon claims 1-2 of the '862 patent and those presently rejected are significant and, with respect, Applicant points out the Office has not met its burden to make clear:

(A) The differences between the inventions defined by the conflicting claims—i.e., the differences between a claim in the patent compared to a claim in the present application; and

(B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim of the present application would have been an obvious variation of the invention defined in a claim in the patent.

See MPEP(II)(B)(1).

As previously stated, Applicant will consider any properly grounded double patenting rejection and will happily provide a terminal disclaimer, if appropriate. However, for completeness, Applicant must note that the Office has not met (and indeed cannot meet) its burden with respect to the present double patenting rejection of claim 19. No other basis for rejection appears in the present Office action. ***Therefore, Applicants respectfully request that the Office acknowledge that claim 19 is allowable.***

Rejection under 35 U.S.C. § 102(b)

Claims 1, 5, 7-11 and 13-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,361,337 to Okin (hereafter "*Okin*"). Applicants respectfully traverse.

Applicants appreciate the general similarity of problems addressed and terminology employed. However, Applicants respectfully note that substantial distinctions exist between the disclosure of *Okin* and the present claims. One such distinction traces to differences in the *stateful* and *stateless* components of the two designs. To highlight that distinction, we turn to the disclosure to *Okin* which clearly establishes that Okin's design is a *stateless* pipeline:

> FIG. 1B is a conceptual block diagram of the state elements and stateless elements of a processor. State elements 2 are coupled to a pipeline 6 over an instruction bus 4. By state elements, the present invention refers to flip-flops and registers on the the [sic] processor chip which store binary information indicative of the state of a particular process or processes. Such state elements typically comprise of register files, status bits, condition codes, and pre-fetched instructions. On the other hand, the pipeline 6 is stateless, i.e. does not store information indicative of the state of process that needs to be preserved during execution of a process.

Okin, col. 3, lines 10-21 (emphasis added).

In contrast, Applicants presently claimed design includes variations on a *stateful* pipeline in which at least some aspects of a thread (or other execution) context are frozen in state elements that exist *in pipeline*. Although each of the independent claims is of different scope, each recites an aspect of this, or a similar, distinction. For example, independent **claim 1** recites:

> a processor that **stores** plural execution contexts **in a pipeline** thereof, the processor performing a context switch between a first one and a second one of the execution contexts by **freezing** the first execution context **in the pipeline** and resuming execution using previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline.

Independent **claim 11** similarly recites:

> performing a context switch between a first one and a second one of the execution contexts by **freezing** the first execution context **in the pipeline** and resuming execution using

> previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline.

Independent **claims 17** and **18** are somewhat similar, reciting:

> means defined in the processor for **storing** plural execution contexts **in a pipeline** thereof, the processor performing a context switch between a first one and a second one of the execution contexts by **freezing** the first execution context **in the pipeline** and resuming execution using previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline,

and

> fabricating the pipelined processor as an integrated circuit with **in-pipeline storage** for plural execution contexts thereof, the in-pipeline storage allowing a context switch between a first one and a second one of the execution contexts by **freezing** the first execution context **in the pipeline** and resuming execution using previously frozen state corresponding to the second execution context, the context switching performable in the fabricated pipelined processor without draining the first execution context from the pipeline,

respectively.

Turning to independent **claim 15**, Applicants positively recite both *in-pipeline* storage for a *stateful* pipeline and a separate register file for context-selectable representation of architectural state. While Applicant's context-selectable register file may arguably correspond to the "state elements" of *Okin* relied upon by the Office, *see Okin*, col. 3, lines 16-18 ("Such state elements typically comprise of register files, status bits, condition codes, and pre-fetched instructions"), Applicant's recital of *in-pipeline* storage for multiple execution contexts does not disclose, and indeed is necessarily inconsistent with *Okin's* disclosure of, a stateless *pipeline*.

For at least the forgoing reasons, each of the independent claims is allowable over *Okin*. Indeed, *Okin* does not disclose or suggest, alone or in combination with any of the applied art, the subject matter of any of the independent claims. Accordingly, claims 1, 11 and 15-18,

together with those that depend therefrom, are all allowable and a notice to that effect is respectfully requested.

Obviousness under 35 U.S.C. §103(a)

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Okin* as applied to claims 1, 5, 7-11 and 13-18, and further in view of U.S. Patent 6,148,395 to Dao et al. (hereafter "*Dao*"). Claims 3-4 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Okin* as applied to claims 1, 5, 7-11 and 13-18, and further in view of *Official Notice*.

Applicants note that all obviousness rejections are necessarily premised on the Office's analysis of *Okin*, which has been addressed above. Since Applicants have rebutted the Office's *Okin*-based positions, and since none of the additional references or teachings relied upon by the Office provide the disclosure missing from *Okin* or otherwise address *Okin*'s deficiencies as applied, no *prima facie* case of obviousness exists. Applicant therefore respectfully requests that all rejections under § 103 be withdrawn.

Conclusion

In summary, claims 1-21 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,

David W. O'Brien, Reg. No. 40,107
Attorney for Applicant(s)
(512) 338-6314 (direct)
(512) 338-6300 (main)
(512) 338-6301 (fax)